ABSTRACT OF THE DISCLOSURE

A method and apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test or scan-test mode, where N > 1 and each domain has a plurality of scan cells. The method and apparatus allows generating and loading N pseudorandom or predetermined stimuli to all the scan cells within the N clock domains in the integrated circuit or circuit assembly during the shift operation, applying an ordered sequence of capture clocks to all the scan cells within the N clock domains during the capture operation, compacting or comparing N output responses of all the scan cells for analysis during the compact/compare operation, and repeating the above process until a predetermined limiting criteria is reached. A computer-aided design (CAD) system is further developed to realize the method and synthesize the apparatus.